R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Trimmings for the indication of allowable matter.

SUPPORT FOR CLAIM AMENDMENTS

Support for amended claims 1 and 10 can be found in the drawings as originally filed, for example, on FIGS. 7-9. As such, no new matter was added.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-4 and 6-10 under 35 U.S.C. §103 as being unpatentable over Scheck in view of the background section is respectfully traversed and should be withdrawn.

Scheck teaches a system and method for reducing clock skew sensitivity of a shift register (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising one or more groups of boundary scan cells, one or more group buffers, one or more repeater buffers, a controller, one or more flip-flops and a scan enable signal. The group buffers may be coupled to each of the groups of boundary scan cells. The repeater buffers may be coupled in series with the group buffers. The controller may be coupled to the groups of boundary scan cells through the group buffers and the repeater buffers. The apparatus may be configured to buffer the groups of boundary scan cells to

reflect an order of I/Os around the apparatus. The groups of boundary scan cells are routed within an I/O portion of the apparatus to avoid routing through an interior portion of the apparatus. The one or more flip-flops may be configured to provide a scan enable output. The scan enable signal may be configured to control a scan connection between each of the flip-flops. Claim 10 provides similar limitations.

The Office Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness (MPEP §2142). Specifically, the Office Action fails to factually establish the suggestion or motivation to modify Scheck as suggested in the Office Action on page 4. The position taken by the Office Action that "one with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the Scheck manner of clock and data distribution" to the background section of routing boundary scan cells with the circuit I/O does not appear to be supported by Scheck (see Office Action page 4, lines 18-20). In particular, the Office Action asserts that the signals shift and mode of Scheck (FIG. 4A shift and mode) is the presently claimed scan enable signal configured to control a scan connection (see Office Action page 6, lines 1-3). However, Scheck fails to describe the operation of the signals shift and mode (FIG. 4A, shift and mode). It is unclear how Scheck teaches the presently claimed scan enable signal. There is nothing in Scheck to support the Office Action's assertion that the signals shift and mode are the presently claimed scan enable signal and the

scan connection. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Moreover, the Applicants have distinguished between a typical scan net flip-flop circuit and the presently claimed apparatus which implements the presently claimed scan enable signal (see specification, pages 12-14). In particular, the Applicants noted that the typical flip-flop circuit of FIG. 6 in the specification included a scan connection (the output Q1) which always switches unnecessarily in functional mode (see specification, page 13, lines 12-15). The Applicants further noted that typical flip-flop implementations consumes too much power and needs additional cooling due to unnecessary switching in the functional mode (see specification, page 13, lines 18-20). As such, the Applicants are able to overcome the deficiencies of the typical flip-flop implementation by implementing the presently claimed scan enable signal configured to control the scan connection (see specification, FIG. 7, page 14, lines 9-11). By controlling the flip-flop with the presently claimed scan enable input and the presently claimed scan enable output (e.g., SEO), the performance of the flip-flop increases (see specification, page 14, lines 3-17). Scheck fails to teach or suggest that the signal shift controls the signal mode to prevent unnecessary switching of flip-flops. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-4 and 6-10 depend, directly or indirectly, from claim 1. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

The rejection of claims 18-20 under 35 U.S.C. §103 as being unpatentable over Scheck in view of the background section has been obviated by appropriate amendment and should be withdrawn. Claim 11 includes the allowable matter of claim 12 and is now believed to be allowable. Claims 18-20 depend, directly or indirectly on the allowable matter of claim 11 and are also believed to be allowable.

As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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